6-Channel, Low Noise, Low Power, 24-Bit Σ-Δ ADC with On-Chip In-Amp and Reference

AD7794

FEATURES

Up to 23 effective bits
RMS noise: 40 nV @ 4.17 Hz
85 nV @ 16.7 Hz
Current: 400 µA typ
Power-down: 1 µA max
Low noise, programmable-gain, instrumentation-amp
Band gap reference with 4 ppm/°C drift typ
Update rate: 4.17 Hz to 500 Hz
Six differential analog inputs
Internal clock oscillator
Simultaneous 50 Hz/60 Hz rejection
Reference detect
Programmable current sources
On-chip bias voltage generator
Burnout currents
Low-side power switch
Power supply: 2.7 V to 5.25 V
–40°C to +105°C temperature range
Independent interface power supply
24-lead TSSOP package

INTERFACE

3-wire serial
SPI®, QSPI™, MICROWIRE™, and DSP compatible
Schmitt trigger on SCLK

APPLICATIONS

Temperature measurement
Pressure measurement
Weigh scales
Strain gauge transducers
Gas analysis
Industrial process control
Instrumentation
Blood analysis
Smart transmitters
Liquid/gas chromatography
6-digit DVM

GENERAL DESCRIPTION

The AD7794 is a low power, low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit Σ-Δ ADC with six differential inputs. The on-chip low noise instrumentation amplifier means that signals of small amplitude can be interfaced directly to the ADC.

The device contains a precision, low noise, low drift internal band gap reference and can also accept up to two external differential references. Other on-chip features include programmable excitation current sources, burnout currents, and a bias voltage generator, which is used to set the common-mode voltage of a channel to $AV_{DD}/2$. The low-side power switch can be used to power down bridge sensors between conversions, minimizing the system's power consumption. The device can be operated with either the internal clock or an external clock. The output data rate from the part can be varied from 4.17 Hz to 500 Hz.

The part operates with a power supply from 2.7 V to 5.25 V. It consumes a current of 400 µA typical and is housed in a 24-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM

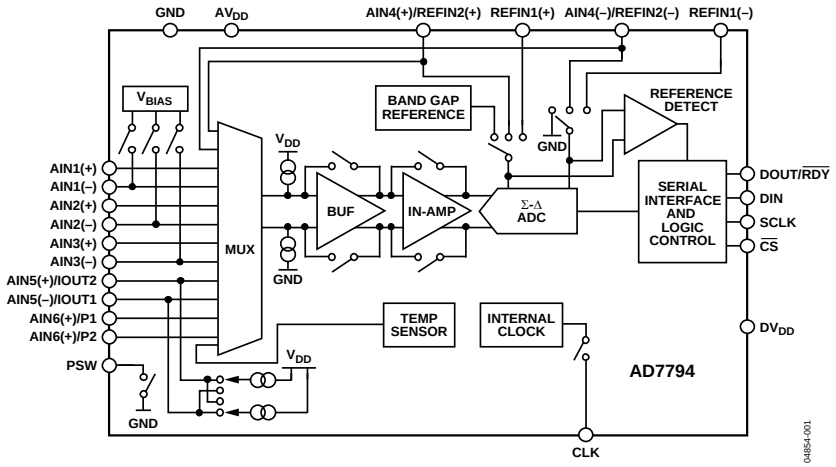

Figure 1.

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10/04—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = 2.7 V to 5.25 V; DV_{DD} = 2.7 V to 5.25 V; GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	AD7794B	Unit	Test Conditions/Comments
AD7794 CHOP ENABLED			
Output Update Rate	4.17 to 500	Hz nom	Settling time = 2/output update rate
No Missing Codes[2]	24	Bits min	$f_{ADC} \leq 250$ Hz
Resolution	See RMS Noise and Resolution Specifications		
RMS Noise and Update Rates	See RMS Noise and Resolution Specifications		
Integral Nonlinearity	±15	ppm of FSR max	
Offset Error[3]	±1	µV typ	
Offset Error Drift vs. Temperature[4]	±10	nV/°C typ	
Full-Scale Error[3, 5]	±10	µV typ	
Gain Drift vs. Temperature[4]	±1	ppm/°C typ	Gain = 1 to 16, external reference
	±3	ppm/°C typ	Gain = 32 to 128, external reference
Power Supply Rejection	100	dB min	AIN = 1 V/gain, gain ≥ 4, external reference
ANALOG INPUTS			
Differential Input Voltage Ranges	± V_{REF}/gain	V nom	V_{REF} = REFIN(+) − REFIN(−) or internal reference, gain = 1 to 128
Absolute AIN Voltage Limits[2]			
Unbuffered Mode	GND − 30 mV	V min	Gain = 1 or 2
	AV_{DD} + 30 mV	V max	
Buffered Mode	GND + 100 mV	V min	Gain = 1 or 2
	AV_{DD} − 100 mV	V max	
In-Amp Active	GND + 300 mV	V min	Gain = 4 to 128
	AV_{DD} − 1.1	V max	
Common-Mode Voltage, V_{CM}	0.5	V min	V_{CM} = (AIN(+) + AIN(−))/2, gain = 4 to 128
Analog Input Current			
Buffered Mode or In-Amp Active			
Average Input Current[2]	±1	nA max	Gain = 1 or 2, update rate < 100 Hz
	±250	pA max	Gain = 4 to 128, update rate < 100 Hz
	±1	nA max	AIN6(+)/AIN6(−)
Average Input Current Drift	±2	pA/°C typ	
Unbuffered Mode			Gain = 1 or 2
Average Input Current	±400	nA/V typ	Input current varies with input voltage
Average Input Current Drift	±50	pA/V/°C typ	
Normal Mode Rejection[2, 6]			
Internal Clock			
@ 50 Hz, 60 Hz	65	dB min	80 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz	80	dB min	90 dB typ, 50 ± 1 Hz, FS[3:0] = 1001
@ 60 Hz	90	dB min	100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000
External Clock			
@ 50 Hz, 60 Hz	80	dB min	90 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz	94	dB min	100 dB typ, 50 ± 1 Hz, FS[3:0] = 1001
@ 60 Hz	90	dB min	100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000
Common-Mode Rejection			
@ DC	100	dB min	AIN = 1 V/gain, gain ≥ 4
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz (FS[3:0] = 1001), 60 ± 1 Hz (FS[3:0] = 1000)

Parameter[1]	AD7794B	Unit	Test Conditions/Comments
AD7794 CHOP DISABLED			
Output Update Rate	4.17 to 500	Hz nom	Settling time = 1/output update rate
No Missing Codes[2]	24	Bits min	f_{ADC} ≤125 Hz
Resolution	See RMS Noise and Resolution Specifications		
RMS Noise and Update Rates	See RMS Noise and Resolution Specifications		
Integral Nonlinearity	±15	ppm of FSR max	
Offset Error[3]	±100/gain	µV typ	Without calibration
Offset Error Drift vs. Temperature[4]	±100/gain	nV/°C typ	Gain = 1 to 16
	10	nV/°C typ	Gain = 32 to 128
Full-Scale Error[3, 5]	±10	µV typ	
Gain Drift vs. Temperature[4]	±1	ppm/°C typ	Gain = 1 to 16, external reference
	±3	ppm/°C typ	Gain = 32 to 128, external reference
Power Supply Rejection	100	dB typ	AIN = 1 V/gain, gain ≥ 4, external reference
ANALOG INPUTS			
Differential Input Voltage Ranges	± V_{REF} /gain	V nom	V_{REF} = REFIN(+) − REFIN(−) or internal reference, gain = 1 to 128
Absolute AIN Voltage Limits[2]			
Unbuffered Mode	GND − 30 mV	V min	Gain = 1 or 2
	AV_{DD} + 30 mV	V max	
Buffered Mode	GND + 100 mV	V min	Gain = 1 or 2
	AV_{DD} − 100 mV	V max	
In-Amp Active	GND + 300 mV	V min	Gain = 4 to 128
	AV_{DD} − 1.1	V max	
Common-Mode Voltage, V_{CM}	0.2 + (gain/2 × (AIN(+) − AIN(-)))	V min	AMP-CM = 1, V_{CM} = (AIN(+) + AIN(−))/2, gain = 4 to 128
	AV_{DD} − 0.2 − (gain/2 × (AIN(+) − AIN(−)))	V max	
Analog Input Current			
Buffered Mode or In-Amp Active			
Average Input Current[2]	±1	nA max	Gain = 1 or 2
	±250	pA max	Gain = 4 to 128
	±1	nA max	AIN6(+)/AIN6(−)
Average Input Current Drift	±2	pA/°C typ	
Unbuffered Mode			Gain = 1 or 2
Average Input Current	±400	nA/V typ	Input current varies with input voltage
Average Input Current Drift	±50	pA/V/°C typ	
Normal Mode Rejection[2, 6]			
Internal Clock			
@ 50 Hz, 60 Hz	60	dB min	70 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz	78	dB min	90 dB typ, 50 ± 1 Hz, FS[3:0] = 1001
@ 60 Hz	86	dB min	100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000
External Clock			
@ 50 Hz, 60 Hz	60	dB min	70 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz	94	dB min	100 dB typ, 50 ± 1 Hz, FS[3:0] = 1001
@ 60 Hz	90	dB min	100 dB typ, 60 ± 1 Hz, FS[3:0] = 1000
Common-Mode Rejection			
@ DC	100	dB min	AIN = 1 V/gain with gain = 4, AMP-CM Bit = 1
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz, 60 ± 1 Hz, FS[3:0] = 1010
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz (FS[3:0] = 1001) 60 ± 1 Hz (FS[3:0] = 1000)

Parameter[1]	AD7794B	Unit	Test Conditions/Comments
AD7794 CHOP ENABLED or DISABLED			
REFERENCE INPUT			
Internal Reference			
Internal Reference Initial Accuracy	1.17 ± 0.01%	V min/max	AV_{DD} = 4 V, T_A = 25°C
Internal Reference Drift[2]	4	ppm/°C typ	
	15	ppm/°C max	
Power Supply Rejection	85	dB typ	
External Reference			
External REFIN Voltage	2.5	V nom	REFIN = REFIN(+) − REFIN(−)
Reference Voltage Range[2]	0.1	V min	
	AV_{DD}	V max	When $V_{REF} = AV_{DD}$, the differential input must be limited to $0.9 \times V_{REF}$/Gain if the in-amp is active
Absolute REFIN Voltage Limits[2]	GND − 30 mV	V min	
	AV_{DD} + 30 mV	V max	
Average Reference Input Current	400	nA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	
Normal Mode Rejection[2]	Same as for analog inputs		
Common-Mode Rejection	100	dB typ	
Reference Detect Levels	0.3	V min	
	0.65	V max	NOXREF bit active if V_{REF} < 0.3 V
EXCITATION CURRENT SOURCES			
(IEXC1 and IEXC2)			
Output Current	10/210/1000	µA nom	
Initial Tolerance at 25°C	±5	% typ	
Drift	200	ppm/°C typ	
Current Matching	±0.5	% typ	Matching between IEXC1 and IEXC2, V_{OUT} = 0 V
Drift Matching	50	ppm/°C typ	
Line Regulation (AV_{DD})	2	%/V typ	AV_{DD} = 5 V ± 5%
Load Regulation	0.2	%/V typ	
Output Compliance	AV_{DD} − 0.65	V max	Current sources programmed to 10 µA or 210 µA
	AV_{DD} − 1.1	V max	Current sources programmed to 1 mA
	GND − 30 mV	V min	
BIAS VOLTAGE GENERATOR			
V_{BIAS}	AV_{DD}/2	V nom	
V_{BIAS} Generator Start-Up Time	See Figure 11	ms/nF typ	Dependent on the capacitance connected to AIN
TEMPERATURE SENSOR			
Accuracy	±2	°C typ	Applies if user calibrates the temp sensor
Sensitivity	0.81	mV/°C typ	
LOW SIDE POWER SWITCH			
R_{ON}	7	Ω max	AV_{DD} = 5 V
	9	Ω max	AV_{DD} = 3 V
Allowable Current[2]	30	mA max	Continuous current
DIGITAL OUTPUTS (P1 and P2)			
V_{OH}, Output High Voltage[2]	AV_{DD} − 0.6	V min	AV_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	AV_{DD} = 3 V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	AV_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	AV_{DD} = 5 V, I_{SINK} = 800 µA
INTERNAL/EXTERNAL CLOCK			
Internal Clock			
Frequency[2]	64 ± 3%	kHz min/max	
Duty Cycle	50:50	% typ	

Parameter[1]	AD7794B	Unit	Test Conditions/Comments
External Clock			
Frequency	64	kHz nom	A 128 kHz external clock can be used if the divide-by-2 function is used (Bit CLK1 = CLK0 = 1)
Duty Cycle	45:55 to 55:45	% typ	Applies for external 64 kHz clock.; a 128 kHz clock can have a less stringent duty cycle
LOGIC INPUTS			
$\overline{CS}$[2]			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	DV_{DD} = 3 V or 5 V
SCLK, CLK and DIN (Schmitt-Triggered Input)[2]			
$V_T(+)$	1.4/2	V min/V max	DV_{DD} = 5 V
$V_T(-)$	0.8/1.7	V min/V max	DV_{DD} = 5 V
$V_T(+) - V_T(-)$	0.1/0.17	V min/V max	DV_{DD} = 5 V
$V_T(+)$	0.9/2	V min/V max	DV_{DD} = 3 V
$V_T(-)$	0.4/1.35	V min/V max	DV_{DD} = 3 V
$V_T(+) - V_T(-)$	0.06/0.13	V min/V max	DV_{DD} = 3 V
Input Currents	±10	µA max	V_{IN} = DV_{DD} or GND
Input Capacitance	10	pF typ	All digital inputs
LOGIC OUTPUT (INCLUDING CLK)			
V_{OH}, Output High Voltage[2]	DV_{DD} − 0.6	V min	DV_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 3 V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	DV_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 5 V, I_{SINK} = 1.6 mA (DOUT/$\overline{RDY}$)/800 µA (CLK)
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset binary		
SYSTEM CALIBRATION[2]			
Full-Scale Calibration Limit	1.05 × FS	V max	
Zero-Scale Calibration Limit	−1.05 × FS	V min	
Input Span	0.8 × FS	V min	
	2.1 × FS	V max	
POWER REQUIREMENTS[7]			
Power Supply Voltage			
AV_{DD} − GND	2.7/5.25	V min/max	
DV_{DD} − GND	2.7/5.25	V min/max	
Power Supply Currents			
I_{DD} Current	140	µA max	110 µA typ @ AV_{DD} = 3 V, 125 µA typ @ AV_{DD} = 5 V, unbuffered mode, external reference
	185	µA max	130 µA typ @ AV_{DD} = 3 V, 165 µA typ @ AV_{DD} = 5 V, buffered mode, gain = 1 or 2, external reference
	400	µA max	300 µA typ @ AV_{DD} = 3 V, 350 µA typ @ AV_{DD} = 5 V, gain = 4 to 128, external reference
	500	µA max	400 µA typ @ AV_{DD} = 3 V, 450 µA typ @ AV_{DD} = 5 V, Gain = 4 to 128, internal reference
I_{DD} (Power-Down Mode)	1	µA max	

[1] Temperature range: −40°C to +105°C.
[2] Specification is not production tested but is supported by characterization data at initial product release.
[3] Following a calibration, this error will be in the order of the noise for the programmed gain and update rate selected.
[4] Recalibration at any temperature will remove these errors.
[5] Full-scale error applies to both positive and negative full-scale and applies at the factory calibration conditions (AV_{DD} = 4 V, gain = 1, T_A = 25°C).
[6] FS[3:0] are the four bits used in the mode register to select the output word rate.
[7] Digital inputs equal to DV_{DD} or GND with excitation currents and bias voltage generator disabled.

TIMING CHARACTERISTICS

AV_{DD} = 2.7 V to 5.25 V; DV_{DD} = 2.7 V to 5.25 V; GND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = DV_{DD}, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
t_3	100	ns min	SCLK high pulse width
t_4	100	ns min	SCLK low pulse width
Read Operation			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_5[5, 6]	10	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	80	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high
Write Operation			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	30	ns min	Data valid to SCLK edge setup time
t_{10}	25	ns min	Data valid to SCLK edge hold time
t_{11}	0	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These numbers are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] SCLK active edge is falling edge of SCLK.
[5] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

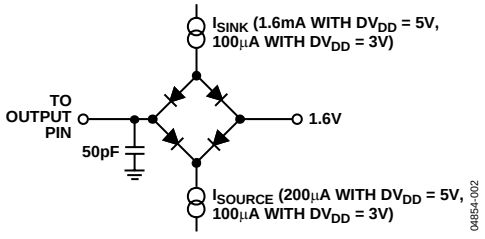

Figure 2. Load Circuit for Timing Characterization

TIMING DIAGRAMS

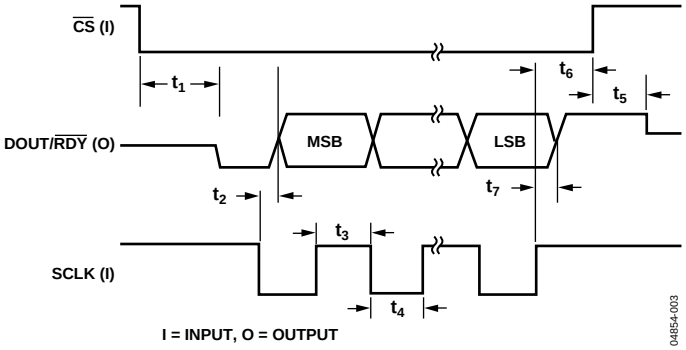

Figure 3. Read Cycle Timing Diagram

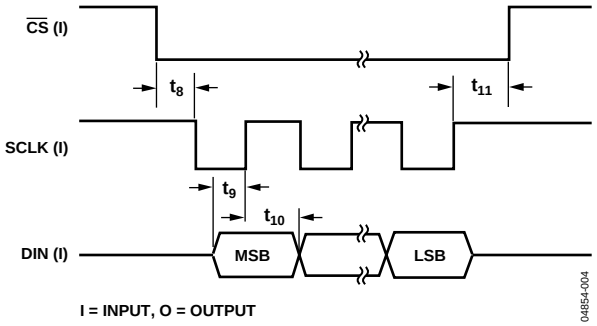

Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +7 V
DV_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
AIN/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP	
θ_{JA} Thermal Impedance	97.9°C/W
θ_{JC} Thermal Impedance	14°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

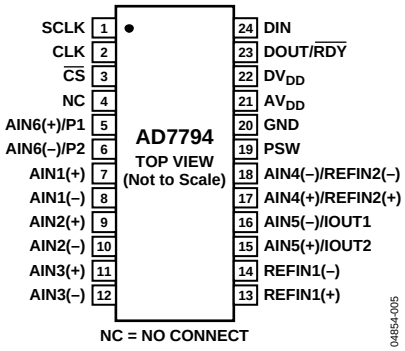

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
2	CLK	Clock In/Clock Out. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. This allows several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed.
3	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.
4	NC	No Connect.
5	AIN6(+)/P1	Analog Input/Digital Output Pin. AIN6(+) is the positive terminal of the differential analog input pair, AIN6(+)/AIN6(–). This pin can also function as a general purpose output bit referenced between AV_{DD} and GND.
6	AIN6(–)/P2	Analog Input/ Digital Output Pin. AIN6(–) is the negative terminal of the differential analog input pair, AIN6(+)/AIN6(–). This pin can also function as a general purpose output bit referenced between AV_{DD} and GND.
7	AIN1(+)	Analog Input. AIN1(+) is the positive terminal of the differential analog input pair, AIN1(+)/AIN1(–).
8	AIN1(–)	Analog Input. AIN1(–) is the negative terminal of the differential analog input pair, AIN1(+)/AIN1(–.
9	AIN2(+)	Analog Input. AIN2(+) is the positive terminal of the differential analog input pair, AIN2(+)/AIN2(–).
10	AIN2(–)	Analog Input. AIN2(–) is the negative terminal of the differential analog input pair, AIN2(+)/AIN2(–).
11	AIN3(+)	Analog Input. AIN3(+) is the positive terminal of the differential analog input pair, AIN3(+)/AIN3(–).
12	AIN3(–)	Analog Input. AIN3(–) is the negative terminal of the differential analog input pair, AIN3(+)/AIN3(–).
13	REFIN1(+)	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(–). REFIN1(+) can lie anywhere between AV_{DD} and GND + 0.1 V. The nominal reference voltage, (REFIN1(+) – REFIN1(–)), is 2.5 V, but the part functions with a reference from 0.1 V to AV_{DD}.
14	REFIN1(–)	Negative Reference Input. This reference input can lie anywhere between GND and AV_{DD} – 0.1 V.
15	AIN5(+)/IOUT2	Analog Input/Output of Internal Excitation Current Source. AIN5(+) is the positive terminal of the differential analog input pair AIN5(+)/AIN5(–). Alternatively, the internal excitation current source can be made available at this pin. The excitation current source is programmable so that the current can be 10 µA, 210 µA or 1 mA. Either IEXC1 or IEXC2 can be switched to this output.
16	AIN5(–)/IOUT1	Analog Input/Output of Internal Excitation Current Source. AIN5(–) is the negative terminal of the differential analog input pair, AIN5(+)/AIN5(–). Alternatively, the internal excitation current source can be made available at this pin and is programmable so that the current can be 10 µA, 210 µA or 1 mA. Either IEXC1 or IEXC2 can be switched to this output.

Pin No.	Mnemonic	Description
17	AIN4(+)/REFIN2(+)	Analog Input/Positive Reference Input. AIN4(+) is the positive terminal of the differential analog input pair AIN4(+)/AIN4(−). This pin can also function as a reference input. REFIN2(+) can lie anywhere between AV_{DD} and GND + 0.1 V. The nominal reference voltage (REFIN2(+) − REFIN2(−)) is 2.5 V, but the part functions with a reference from 0.1 V to AV_{DD}.
18	AIN4(−)/REFIN2(−)	Analog Input/Negative Reference Input. AIN4(−) is the negative terminal of the differential analog input pair AIN4(+)/AIN4(−). This pin also functions as the negative reference input for REFIN2. This reference input can lie anywhere between GND and AV_{DD} − 0.1 V.
19	PSW	Low-Side Power Switch to GND.
20	GND	Ground Reference Point.
21	AV_{DD}	Supply Voltage, 2.7 V to 5.25 V.
22	DV_{DD}	Serial Interface Supply Voltage, 2.7 V to 5.25 V. DV_{DD} is independent of AV_{DD}. Therefore, the serial interface can be operated at 3 V with AV_{DD} at 5 V or vice versa.
23	DOUT/$\overline{\text{RDY}}$	Serial Data Output/Data Ready Output. DOUT/$\overline{\text{RDY}}$serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{\text{RDY}}$operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin will go high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{\text{RDY}}$ pin. With $\overline{\text{CS}}$ low, the data/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.
24	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC, the register selection bits of the communications register identifying the appropriate register.

RMS NOISE AND RESOLUTION SPECIFICATIONS

The AD7794 can be operated with chopping enabled or chopping disabled, allowing the ADC to be optimized for switching time or optimized for drift performance. With chopping enabled, the settling time is two times the conversion time. However, the offset is continuously removed by the ADC leading to low offset and low offset drift. With chopping disabled, the allowable update rates are the same as in chop enable mode. However, the settling time now equals the conversion time. With chopping disabled, the offset is not removed by the ADC, so periodic offset calibrations may be required to remove offset due to drift.

CHOPPING ENABLED

External Reference

Table 5 shows the AD7794's rms noise for some of the update rates and gain settings. The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table **6** shows the effective resolution, while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there will be no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 5. RMS Noise (μV) vs. Gain and Output Update Rate Using an External 2.5 V Reference with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	0.64	0.6	0.29	0.22	0.1	0.065	0.039	0.041
8.33	1.04	0.96	0.38	0.26	0.13	0.078	0.057	0.055
16.7	1.55	1.45	0.54	0.36	0.18	0.11	0.087	0.086
33.3	2.3	2.13	0.74	0.5	0.23	0.17	0.124	0.118
62.5	2.95	2.85	0.92	0.58	0.29	0.2	0.153	0.144
125	4.89	4.74	1.49	1	0.48	0.32	0.265	0.283
250	11.76	9.5	4.02	1.96	0.88	0.45	0.379	0.397
500	11.33	9.44	3.07	1.79	0.99	0.63	0.568	0.593

Table 6. Typical Resolution (Bits) vs. Gain and Output Update Rate Using an External 2.5 V Reference with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	23 (20.5)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	20 (17.5)
8.33	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	21 (18.5)	20.5 (18)	19.5 (17)
16.7	21.5 (19)	20.5 (18)	21 (18.5)	20.5 (18)	20.5 (18)	20.5 (18)	20 (17.5)	19 (16.5)
33.3	21 (18.5)	20 (17.5)	20.5 (18)	20 (17.5)	20.5 (18)	20 (17.5)	19 (16.5)	18.5 (16)
62.5	20.5 (18)	19.5 (17)	20.5 (18)	20 (17.5)	20 (17.5)	19.5 (17)	19 (16.5)	18 (15.5)
125	20 (17.5)	19 (16.5)	19.5 (17)	19 (16.5)	19.5 (17)	19 (16.5)	18 (15.5)	17 (14.5)
250	18.5 (16)	18 (15.5)	18 (15.5)	18 (15.5)	18.5 (16)	18.5 (16)	17.5 (15)	16.5 (14)
500	18.5 (16)	18 (15.5)	18.5 (16)	18.5 (16)	18 (15.5)	18 (15.5)	17 (14.5)	16 (13.5)

Internal Reference

Table 7 shows the AD7794's rms noise for some of the update rates and gain settings. The numbers given are for the bipolar input range with the internal 1.17 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 8 shows the effective resolution while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there will be no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 7. RMS Noise (μV) vs. Gain and Output Update Rate (Internal Reference) with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	0.81	0.67	0.32	0.2	0.13	0.065	0.04	0.039
8.33	1.18	1.11	0.41	0.25	0.16	0.078	0.058	0.059
16.7	1.96	1.72	0.55	0.36	0.25	0.11	0.088	0.088
33.3	2.99	2.48	0.83	0.48	0.33	0.17	0.13	0.12
62.5	3.6	3.25	1.03	0.65	0.46	0.2	0.15	0.15
125	5.83	5.01	1.69	0.96	0.67	0.32	0.25	0.26
250	11.22	8.64	2.69	1.9	1.04	0.45	0.35	0.34
500	12.46	10.58	4.58	2	1.27	0.63	0.50	0.49

Table 8. Typical Resolution (Bits) vs. Gain and Output Update Rate (Internal Reference) with Chop Enabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	21.5 (19)	20.5 (18)	21 (18.5)	20.5 (18)	20 (17.5)	20 (17.5)	20 (17.5)	19 (16.5)
8.33	21 (18.5)	20 (17.5)	20.5 (18)	20 (17.5)	20 (17.5)	20 (17.5)	19 (16.5)	18 (15.5)
16.7	20 (17.5)	19.5 (17)	20 (17.5)	19.5 (17)	19 (16.5)	19.5 (17)	18.5 (16)	17.5 (15)
33.3	19.5 (17)	19 (16.5)	19.5 (17)	19 (16.5)	19 (16.5)	18.5 (16)	18 (15.5)	17 (14.5)
62.5	19.5 (17)	18.5 (16)	19 (16.5)	19 (16.5)	18.5 (16)	18.5 (16)	18 (15.5)	17 (14.5)
125	18.5 (16)	18 (15.5)	18.5 (16)	18 (15.5)	17.5 (15)	18 (15.5)	17 (14.5)	16 (13.5)
250	17.5 (15)	17 (14.5)	17.5 (15)	17 (14.5)	17 (14.5)	17.5 (15)	16.5 (14)	15.5 (13)
500	17.5 (15)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	16 (13.5)	15 (12.5)

CHOPPING DISABLED

With chopping disabled, the switching time or settling time is reduced by a factor of two. However, periodic offset calibrations may now be required to remove offset and offset drift. When chopping is disabled, the AMP-CM bit in the mode register should be set to 1. This limits the allowable common-mode voltage that can be used. However, the common-mode rejection will degrade if the bit is not set.

Table 9 shows the rms noise of the AD7794 for some of the update rates and gain settings with chopping disabled. The numbers given are for the bipolar input range with the internal 1.17 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 10 shows the effective resolution while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there will be no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 9. RMS Noise (μV) vs. Gain and Output Update Rate Using the Internal Reference with Chop Disabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	1.22	0.98	0.33	0.18	0.13	0.062	0.053	0.051
8.33	1.74	1.53	0.49	0.29	0.21	0.1	0.079	0.07
16.7	2.64	2.44	0.79	0.48	0.33	0.16	0.13	0.12
33.3	4.55	3.52	1.11	0.66	0.46	0.21	0.17	0.16
62.5	5.03	4.45	1.47	0.81	0.58	0.27	0.2	0.22
125	8.13	7.24	2.27	1.33	0.96	0.48	0.36	0.37
250	15.12	13.18	3.77	2.09	1.45	0.64	0.5	0.47
500	17.18	14.63	8.86	2.96	1.92	0.89	0.69	0.7

Table 10. Typical Resolution (Bits) vs. Gain and Output Update Rate Using the Internal Reference with Chop Disabled

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17	21 (18.5)	20 (17.5)	21 (18.5)	20.5 (18)	20 (17.5)	20 (17.5)	19.5 (17)	18.5 (16)
8.33	20.5 (18)	19.5 (17)	20 (17.5)	20 (17.5)	19.5 (17)	19.5 (17)	19 (16.5)	18 (15.5)
16.7	20 (17.5)	19 (16.5)	19.5 (17)	19 (16.5)	19 (16.5)	19 (16.5)	18 (15.5)	17 (14.5)
33.3	19 (16.5)	18.5 (16)	19 (16.5)	19 (16.5)	18.5 (16)	18.5 (16)	17.5 (15)	17 (14.5)
62.5	19 (16.5)	18 (15.5)	18.5 (16)	18.5 (16)	18 (15.5)	18 (15.5)	17.5 (15)	16.5 (14)
125	18 (15.5)	17.5 (15)	18 (15.5)	17.5 (15)	17 (14.5)	17 (14.5)	16.5 (14)	15.5 (13)
250	17 (14.5)	16.5 (14)	17 (14.5)	17 (14.5)	16.5 (14)	17 (14.5)	16 (13.5)	15 (12.5)
500	17 (14.5)	16.5 (14)	16 (13.5)	16.5 (14)	16 (13.5)	16.5 (14)	15.5 (13)	14.5 (12)

TYPICAL PERFORMANCE CHARACTERISTICS

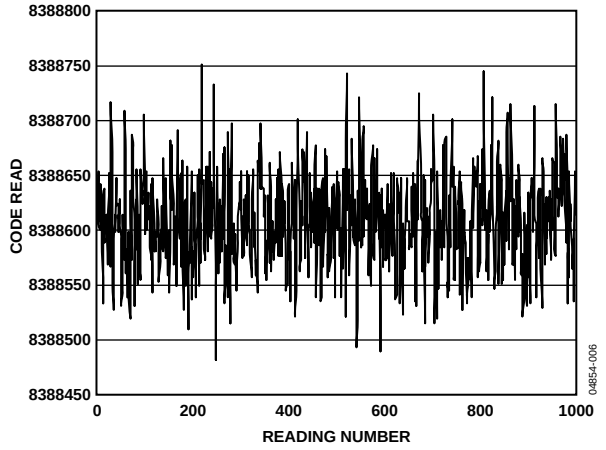

Figure 6. Typical Noise Plot (Internal Reference, Gain = 64, Update Rate = 16.7 Hz, Chop Enabled)

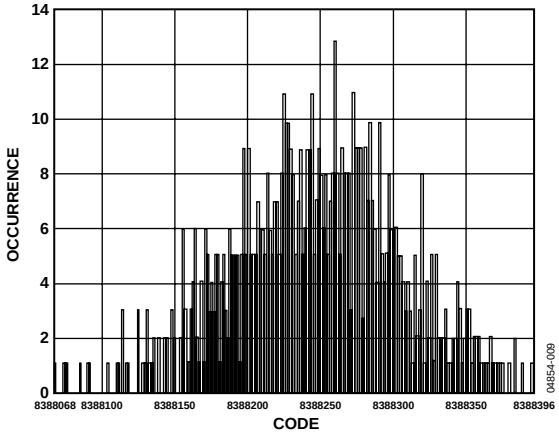

Figure 9. Noise Distribution Histogram (Internal Reference, Gain = 64, Update Rate = 16.7 Hz, Chop Disabled, AMP-CM = 1)

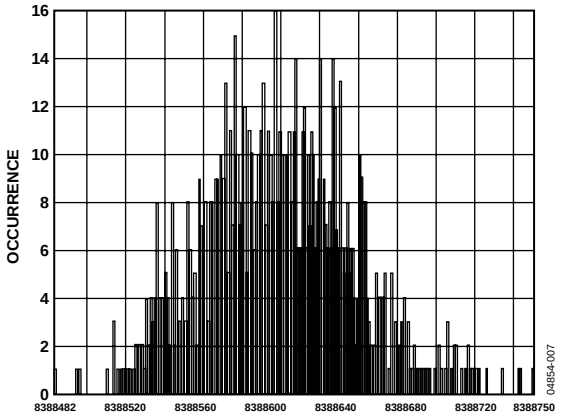

Figure 7. Noise Distribution Histogram (Internal Reference, Gain = 64, Update Rate = 16.7 Hz, Chop Enabled)

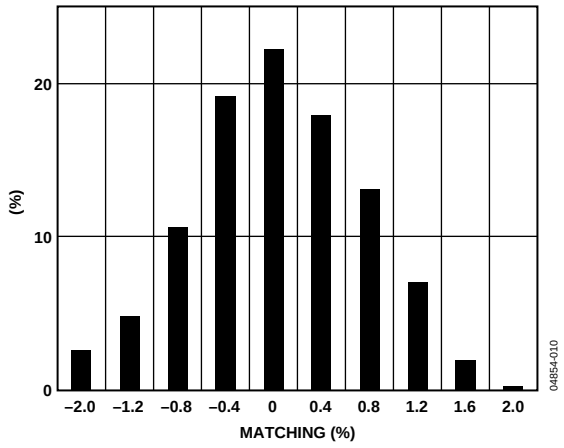

Figure 10. Excitation Current Matching (210 µA) at Ambient Temperature

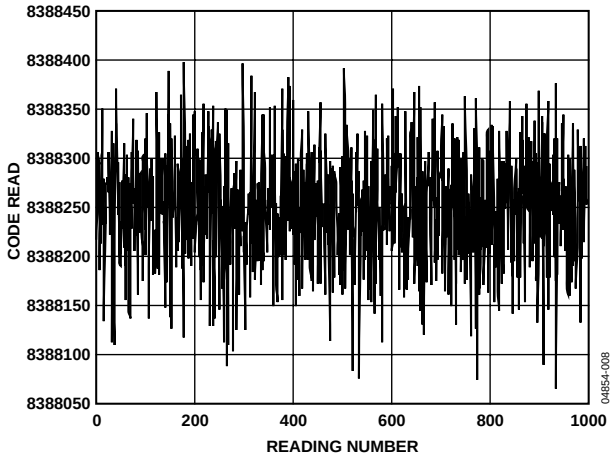

Figure 8. Typical Noise Plot when Gain = 64 and Internal Reference Selected (Chop Disabled, AMP-CM = 1)

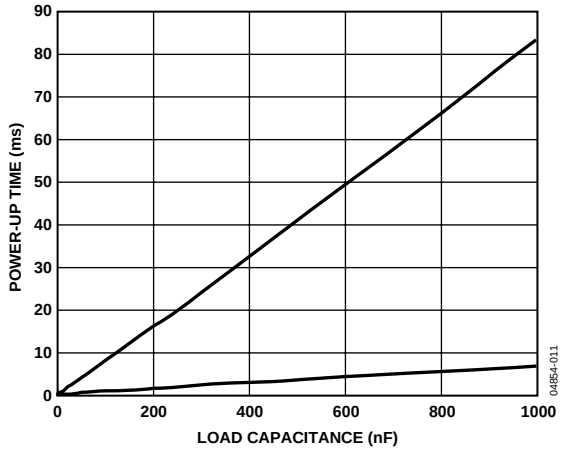

Figure 11. Bias Voltage Generator Power Up Time vs. Load Capacitance

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise noted.

COMMUNICATIONS REGISTER

(RS2, RS1, RS0 = 0, 0, 0)

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 11 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	R/$\overline{\text{W}}$(0)	RS2(0)	RS1(0)	RS0(0)	CREAD(0)	0(0)	0(0)

Table 11. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the communications register.
CR6	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation will be a write to a specified register. A 1 in this position indicates that the next operation will be a read from the designated register.
CR5 to CR3	RS2 to RS0	Register Address Bits. These address bits are used to select which registers of the ADC are being selected during this serial interface communication. See Table 12.
CR2	CREAD	Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read, that is, the contents of the data register are automatically placed on the DOUT pin when the SCLK pulses are applied after the $\overline{\text{RDY}}$ pin goes low to indicate that a conversion is complete. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 01011100 must be written to the communications register. To exit the continuous read mode, the instruction 01011000 must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.
CR1 to CR0	0	These bits must be programmed to Logic 0 for correct operation.

Table 12. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register During a Write Operation	8-bit
0	0	0	Status Register During a Read Operation	8-bit
0	0	1	Mode Register	16-bit
0	1	0	Configuration Register	16-bit
0	1	1	Data Register	24-bit
1	0	0	ID Register	8-bit
1	0	1	IO Register	8-bit
1	1	0	Offset Register	24-bit
1	1	1	Full-Scale Register	24-bit

STATUS REGISTER

(RS2, RS1, RS0 = 0, 0, 0; Power-On/Reset = 0x88)

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load Bit RS2, Bit RS1, and Bit RS0 with 0. Table 13 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, SR denoting the bits are in the status register. SR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{\text{RDY}}$(1)	ERR(0)	NOREF(0)	0(0)	1(1)	CH2(0)	CH1(0)	CH0(0)

Table 13. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{\text{RDY}}$	Ready Bit for ADC. *Cleared* when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also set when the part is placed in power-down mode. The end of a conversion is also indicated by the DOUT/$\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC Error Bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. *Set* to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange, underrange, or the absence of a reference voltage. *Cleared* by a write operation to start a conversion.
SR5	NOREF	No External Reference Bit. *Set* to indicate that the selected reference (REFIN1 or REFIN2) is at a voltage that is below a specified threshold. When set, conversion results are clamped to all ones. *Cleared* to indicate that a valid reference is applied to the selected reference pins. The NOXREF bit is enabled by setting the REF_DET bit in the configuration register to 1. The ERR bit is also set if the voltage applied to the selected reference input is invalid.
SR4	0	This bit is automatically *cleared*.
SR3	1	This bit is automatically *set*.
SR2 to SR0	CH2 to CH0	These bits indicate which channel is being converted by the ADC.

MODE REGISTER

(RS2, RS1, RS0 = 0, 0, 1; Power-On/Reset = 0x000A)

The mode register is a 16-bit register from which data can be read or to which data can be written. This register is used to select the operating mode, the update rate, and the clock source. Table 14 outlines the bit designations for the mode register. MR0 through MR15 indicate the bit locations, MR denoting the bits are in the mode register. MR15 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter and sets the $\overline{\text{RDY}}$ bit.

MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8
MD2(0)	MD1(0)	MD0(0)	PSW(0)	0(0)	0(0)	AMP-CM(0)	0(0)
MR7	**MR6**	**MR5**	**MR4**	**MR3**	**MR2**	**MR1**	**MR0**
CLK1(0)	CLK0(0)	0(0)	CHOP-DIS(0)	FS3(1)	FS2(0)	FS1(1)	FS0(0)

Table 14. Mode Register Bit Designations

Bit Location	Bit Name	Description
MR15 to MR13	MD2 to MD0	Mode Select Bits. These bits select the operational mode of the AD7794 (see Table 15).
MR12	PSW	Power Switch Control Bit. *Set* by user to close the power switch PSW to GND. The power switch can sink up to 30 mA. *Cleared* by user to open the power switch. When the ADC is placed in power-down mode, the power switch is opened.
MR11 to MR10	0	These bits must be programmed with a Logic 0 for correct operation.
MR9	AMP-CM	Instrumentation Amplifier Common-Mode Bit. It is used in conjunction with the CHOP-DIS bit. When chopping is disabled, the user can operate with a wider range of common-mode voltages when AMP-CM is cleared. However, the dc common-mode rejection will degrade. With AMP-CM set, the span for the common-mode voltage is reduced (see Specifications section). However, the dc common-mode rejection is significantly better.

Bit Location	Bit Name	Description		
MR8	0	This bit must be programmed with a Logic 0 for correct operation.		
MR7 to MR6	CLK1 to CLK0	These bits are used to select the clock source for the AD7794. Either the on-chip 64 kHz clock can be used or an external clock can be used. The ability to use an external clock allows several AD7794 devices to be synchronized. Also, 50 Hz/60 Hz rejection is improved when an accurate external clock drives the AD7794.		
		CLK1	**CLK0**	**ADC Clock Source**
		0	0	Internal 64 kHz clock. Internal clock is not available at the CLK pin
		0	1	Internal 64 kHz clock. This clock is made available at the CLK pin
		1	0	External 64 kHz clock used. The external clock can have a 45:55 duty cycle. See specifications for external clock.
		1	1	External clock used. The external clock is divided by 2 within the AD7794.
MR5	0	This bit must be programmed with a Logic 0 for correct operation.		
MR4	CHOP-DIS	This bit is used to enable or disable chopping. On power-up or following a reset, CHOP-DIS is *cleared* so chopping is enabled. When CHOP-DIS is *set*, chopping is disabled. This bit is used in conjunction with the AMP-CM bit. When chopping is disabled, the AMP-CM bit should be *set*. This will limit the common mode voltage which can be used by the ADC but the dc common-mode rejection will not degrade.		
MR3 to MR0	FS3 to FS0	Filter Update Rate Select Bits (see Table 16).		

Table 15. Operating Modes

MD2	MD1	MD0	Mode
0	0	0	Continuous Conversion Mode (Default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. $\overline{RDY}$ goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, the first conversion is available after a period $2/f_{ADC}$ when chopping is enabled or $1/f_{ADC}$ when chopping is disabled. Subsequent conversions are available at a frequency of f_{ADC} with chopping either enabled or disabled.
0	0	1	Single Conversion Mode. When single conversion mode is selected, the ADC powers up and performs a single conversion. The oscillator requires 1 ms to power up and settle. The ADC then performs the conversion which takes a time of $2/f_{ADC}$ when chopping is enabled or $1/f_{ADC}$ when chopping is disabled. The conversion result is placed in the data register, $\overline{RDY}$ goes low, and the ADC returns to power-down mode. The conversion remains in the data register and $\overline{RDY}$ remains active (low) until the data is read or another conversion is performed.
0	1	0	Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided.
0	1	1	Power-Down Mode. In power-down mode, all the AD7794 circuitry is powered down including the current sources, power switch, burnout currents, bias voltage generator, and CLKOUT circuitry.
1	0	0	Internal Zero-Scale Calibration. An internal short is automatically connected to the enabled channel. A calibration takes two conversion cycles to complete when chopping is enabled and one conversion cycle when chopping is disabled. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	0	1	Internal Full-Scale Calibration. A full-scale input voltage is automatically connected to the selected analog input for this calibration. When the gain equals 1, a calibration takes two conversion cycles to complete when chopping is enabled and one conversion cycle when chopping is disabled. For higher gains, four conversion cycles are required to perform the full-scale calibration when chopping is enabled and 2 conversion cycles when chopping is disabled. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. Internal full-scale calibrations cannot be performed when the gain equals 128. With this gain setting, a system full-scale calibration can be performed. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.

MD2	MD1	MD0	Mode
1	1	0	System Zero-Scale Calibration. User should connect the system zero-scale input to the channel input pins as selected by the CH2 to CH0 bits. A system offset calibration takes 2 conversion cycles to complete when chopping is enabled and one conversion cycle when chopping is disabled. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	1	1	System Full-Scale Calibration. User should connect the system full-scale input to the channel input pins as selected by the CH2–CH0 bits. A calibration takes 2 conversion cycles to complete when chopping is enabled and one conversion cycle when chopping is disabled. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed.

Table 16. Update Rates Available (Chopping Enabled)

FS3	FS2	FS1	FS0	f_{ADC} (Hz)	T_{SETTLE} (ms)	Rejection @ 50 Hz/60 Hz (Internal Clock)
0	0	0	0	x	x	
0	0	0	1	500	4	
0	0	1	0	250	8	
0	0	1	1	125	16	
0	1	0	0	62.5	32	
0	1	0	1	50	40	
0	1	1	0	39.2	48	
0	1	1	1	33.3	60	
1	0	0	0	19.6	101	90 dB (60 Hz only)
1	0	0	1	16.7	120	80 dB (50 Hz only)
1	0	1	0	16.7	120	65 dB (50 Hz and 60 Hz)
1	0	1	1	12.5	160	66 dB (50 Hz and 60 Hz)
1	1	0	0	10	200	69 dB (50 Hz and 60 Hz)
1	1	0	1	8.33	240	70 dB (50 Hz and 60 Hz)
1	1	1	0	6.25	320	72 dB (50 Hz and 60 Hz)
1	1	1	1	4.17	480	74 dB (50 Hz and 60 Hz)

With chopping disabled, the update rates remain unchanged, but the settling time for each update rate is reduced by a factor of 2. The rejection at 50 Hz/60 Hz for a 16.6 Hz update rate degrades to 60 dB.

CONFIGURATION REGISTER

(RS2, RS1, RS0 = 0, 1, 0; Power-On/Reset = 0x0710)

The configuration register is a 16-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode, enable or disable the buffer, enable or disable the burnout currents, select the gain, and select the analog input channel.

Table 17 outlines the bit designations for the filter register. CON0 through CON15 indicate the bit locations. CON denotes that the bits are in the configuration register. CON15 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

CON15	CON14	CON13	CON12	CON11	CON10	CON9	CON8
VBIAS1(0)	VBIAS0(0)	BO(0)	U/$\overline{B}$(0)	BOOST(0)	G2(1)	G1(1)	G0(1)
CON7	**CON6**	**CON5**	**CON4**	**CON3**	**CON2**	**CON1**	**CON0**
REFSEL1(0)	REFSEL0(0)	REF_DET(0)	BUF(1)	CH3(0)	CH2(0)	CH1(0)	CH0(0)

Table 17. Configuration Register Bit Designations

Bit Location	Bit Name	Description
CON15 to CON14	VBIAS1 to VBIAS0	Bias Voltage Generator Enable. The negative terminal of the analog inputs can be biased up to $AV_{DD}/2$. These bits are used in conjunction with the BOOST bit.

VBIAS1	VBIAS0	Bias Voltage
0	0	Bias voltage generator disabled
0	1	Bias voltage generator connected to AIN1(–
1	0	Bias voltage generator connected to AIN2(–)
1	1	Bias voltage generator connected to AIN3(–)

CON13	BO	Burnout Current Enable Bit. This bit must be programmed with a Logic 0 for correct operation. When this bit is set to 1 by the user, the 100 nA current sources in the signal path are enabled. When BO = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer or in-amp is active.
CON12	U/$\overline{B}$	Unipolar/Bipolar Bit. *Set* by user to enable unipolar coding, that is, zero differential input will result in 0x000000 output and a full-scale differential input will result in 0xFFFFFF output. *Cleared* by the user to enable bipolar coding. Negative full-scale differential input will result in an output code of 0x000000, zero differential input will result in an output code of 0x800000, and a positive full-scale differential input will result in an output code of 0xFFFFFF.
CON11	BOOST	This bit is used in conjunction with the VBIAS1 and VBIAS0 bits. When *set*, the current consumed by the bias voltage generator is increased, which reduces its power-up time.
CON10 to CON8	G2 to G0	Gain Select Bits. Written by the user to select the ADC input range as follows:

G2	G1	G0	Gain	ADC Input Range (2.5 V Reference)
0	0	0	1 (in-amp not used)	2.5 V
0	0	1	2 (in-amp not used)	1.25 V
0	1	0	4	625 mV
0	1	1	8	312.5 mV
1	0	0	16	156.2 mV
1	0	1	32	78.125 mV
1	1	0	64	39.06 mV
1	1	1	128	19.53 mV

CON7 to CON6	REFSEL1/REFSEL0	Reference Select Bits. The reference source for the ADC is selected using these bits.

REFSEL1	REFSEL0	Reference Source
0	0	External reference applied between REFIN1(+) and REFIN1(–)
0	1	External reference applied between REFIN2(+) and REFIN2(–)
1	0	Internal 1.17 V reference
1	1	Reserved

CON5	REF_DET	Enables the Reference Detect Function. When *set*, the NOXREF bit in the status register indicates when the external reference being used by the ADC is open circuit or less than 0.5 V. When *cleared*, the reference detect function is disabled.
CON4	BUF	Configures the ADC for buffered or unbuffered mode of operation. If *cleared*, the ADC operates in unbuffered mode, lowering the power consumption of the device. If *set*, the ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system. For gains of 1 and 2, the buffer can be enabled or disabled. For higher gains, the buffer is automatically enabled. With the buffer disabled, the voltage on the analog input pins can be from 30 mV below GND to 30 mV above AV_{DD}. When the buffer is enabled, it requires some headroom so the voltage on any input pin must be limited to 100 mV within the power supply rails.

Bit Location	Bit Name	Description					
CON3 to CON0	CH3 to CH0	Channel Select Bits. Written by the user to select the active analog input channel to the ADC.					
		CH3	**CH2**	**CH1**	**CH0**	**Channel**	**Calibration Pair**
		0	0	0	0	AIN1(+) – AIN1(–)	0
		0	0	0	1	AIN2(+) – AIN2(–)	1
		0	0	1	0	AIN3(+) – AIN3(–)	2
		0	0	1	1	AIN4(+) – AIN4(–)	3
		0	1	0	0	AIN5(+) – AIN5(–)	3
		0	1	0	1	AIN6(+) – AIN6(–)	3
		0	1	1	0	Temp Sensor	Automatically selects the internal reference and sets the gain to 1
		0	1	1	1	AV_{DD} Monitor	Automatically selects the internal 1.17 V reference and sets the gain to 1/6
		1	0	0	0	AIN1(–) – AIN1(–)	0
		1	0	0	1	Reserved	
		1	0	1	1	Reserved	
		1	1	0	0	Reserved	
		1	1	0	1	Reserved	
		1	1	1	0	Reserved	
		1	1	1	1	Reserved	

DATA REGISTER

(RS2, RS1, RS0 = 0, 1, 1; Power-On/Reset = 0x000000)

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the $\overline{RDY}$ bit/pin is set.

ID REGISTER

(RS2, RS1, RS0 = 1, 0, 0; Power-On/Reset = 0xXF)

The identification number for the AD7794 is stored in the ID register. This is a read-only register.

IO REGISTER

(RS2, RS1, RS0 = 1, 0, 1; Power-On/Reset = 0x00)

The IO register is an 8-bit register from which data can be read or to which data can be written. This register is used to enable the excitation currents and select the value of the excitation currents.

Table 18 outlines the bit designations for the IO register. IO0 through IO7 indicate the bit locations. IO denotes that the bits are in the IO register. IO7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
0(0)	IOEN(0)	IO2DAT(0)	IO1DAT(0)	IEXCDIR1(0)	IEXCDIR0(0)	IEXCEN1(0)	IEXCEN0(0)

Table 18. IO Register Bit Designations

Bit Location	Bit Name	Description		
IO7	0	This bit must be programmed with a Logic 0 for correct operation.		
IO6	IOEN	Configures Pin AIN6(+)/P2 and Pin AIN6(–)/P2 as analog input pins or digital output pins. When this bit is set, the pins are configured as Digital Output Pin P1 and Digital Output Pin P2. When this bit is *cleared*, these pins are configured as Analog Input Pin AIN6(+) and Analog Input Pin AIN6(–).		
IO5 to IO4	IO2DAT/IO1DAT	P2/P1 Data. When IOEN is set, the data for Digital Output Pin P1 and Digital Output Pin P2 is written to Bit IO2DAT and Bit IO1DAT.		
IO3 to IO2	IEXCDIR1 to IEXCDIR0	Direction of Current Sources Select Bits.		
		EXCDIR1	**IEXCDIR0**	**IEXCDIR0**
		0	0	Current Source IEXC1 connected to Pin IOUT1. Current Source IEXC2 connected to Pin IOUT2.
		0	1	Current Source IEXC1 connected to Pin IOUT2. Current Source IEXC2 connected to Pin IOUT1.
		1	0	Both current sources connected to Pin IOUT1. Permitted only when the current sources are set to 10 µA or 210 µA.
		1	1	Both current sources connected to Pin IOUT2. Permitted only when the current sources are set to 10 µA or 210 µA.
IO3 to IO2	IEXCEN1 to IEXCEN0	These bits are used to enable and disable the current sources along with selecting the value of the excitation currents.		
		IEXCEN1	**IEXCEN0**	**Current Source Value**
		0	0	Excitation currents disabled
		0	1	10 µA
		1	0	210 µA
		1	1	1 mA

OFFSET REGISTER

(RS2, RS1, RS0 = 1, 1, 0; Power-On/Reset = 0x800000)

The offset register holds the offset calibration coefficient for the ADC. The power-on reset value of the offset register is 0x800000. The AD7794 has four offset registers. Channel AIN1 to Channel AIN3 have dedicated offset registers while the AIN4, AIN5 and AIN6 channels share an offset register. Each of these registers is a 24-bit read/write register. This register is used in conjunction with its associated full-scale register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The AD7794 must be placed in power-down mode or idle mode when writing to the offset register.

FULL-SCALE REGISTER

(RS2, RS1, RS0 = 1, 1, 1; Power-On/Reset = 0x5XXX00)

The full-scale register is a 24-bit register that holds the full-scale calibration coefficient for the ADC. The AD7794 has 4 full-scale registers. The AIN1, AIN2 and AIN3 channels have dedicated full-scale registers, while the AIN4, AIN5, and AIN6 channels share a register. The full-scale registers are read/write registers. However, when writing to the full-scale registers, the ADC must be placed in power-down mode or idle mode. These registers are configured on power-on with factory-calibrated full-scale calibration coefficients, the calibration being performed at gain = 1. Therefore, every device will have different default coefficients. The coefficients are different, depending on whether the internal reference or an external reference is selected. The default value will be automatically overwritten if an internal or system full-scale calibration is initiated by the user or the full-scale register is written to.

ADC CIRCUIT INFORMATION

OVERVIEW

The AD7794 is a low power ADC that incorporates a Σ-Δ modulator, a buffer, reference, in-amp, and on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in pressure transducers, weigh scales, and temperature measurement applications.

The part has six differential inputs that can be buffered or unbuffered. The device can be operated with the internal 1.17 V reference or an external reference can be used. Figure 12 shows the basic connections required to operate the part.

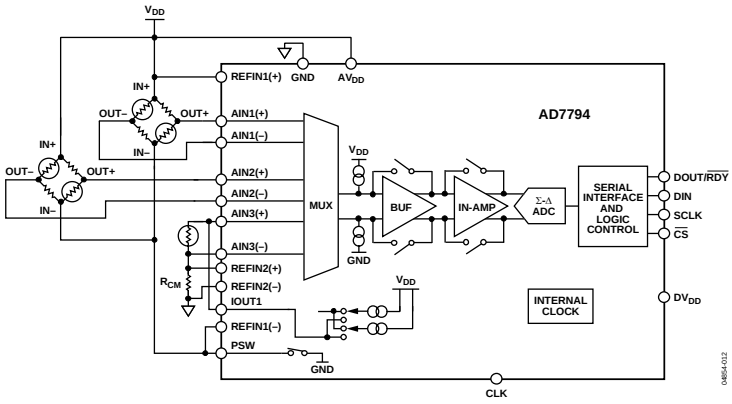

Figure 12. Basic Connection Diagram

The output rate of the AD7794 (f_{ADC}) is user programmable. The allowable update rates, along with the corresponding settling times, are listed in Table 16 for chop enabled. With chop disabled, the allowable update rates remain unchanged, but the settling time equals $1/f_{ADC}$. Normal mode rejection is the major function of the digital filter. Simultaneous 50 Hz and 60 Hz rejection is optimized when the update rate equals 16.7 Hz or less, as notches are placed at both 50 Hz and 60 Hz with these update rates (see Figure 14).

The AD7794 uses slightly different filter types, depending on the output update rate, so that the rejection of quantization noise and device noise is optimized. When the update rate is from 4.17 Hz to 12.5 Hz, a Sinc3 filter along with an averaging filter is used. When the update rate is from 16.7 Hz to 39.2 Hz, a modified Sinc3 filter is used. This filter gives simultaneous 50 Hz/60 Hz rejection when the update rate equals 16.7 Hz. A Sinc4 filter is used when the update rate is from 50 Hz to 250 Hz. Finally, an integrate-only filter is used when the update rate equals 500 Hz. Figure 13 to Figure 16 show the frequency response of the different filter types for some of the update rates when chopping is enabled. In this mode, the settling time equals twice the update rate. Figure 17 to Figure 20 show the filter response with chopping disabled.

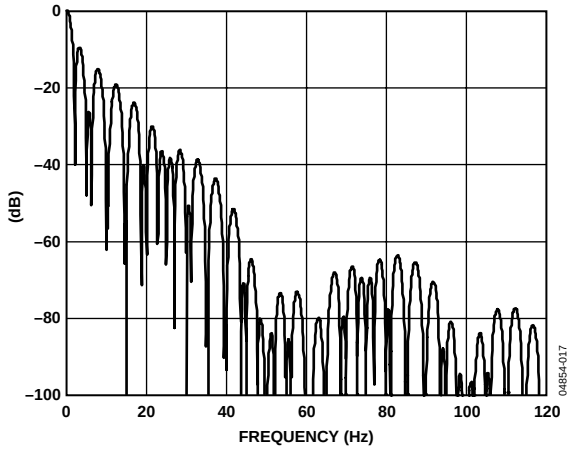

Figure 13. Filter Profile with Update Rate = 4.17 Hz (Chop Enabled)

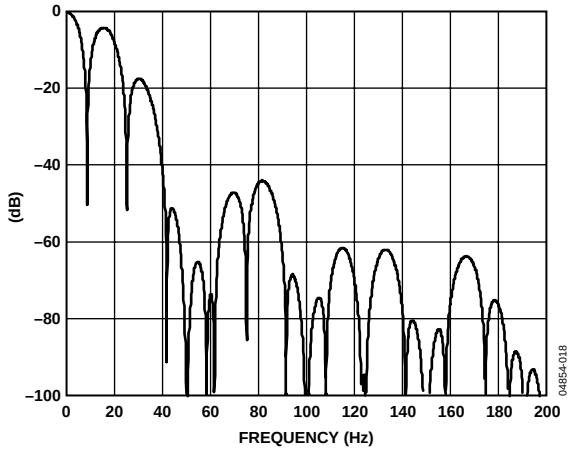

Figure 14. Filter Profile with Update Rate = 16.7 Hz (Chop Enabled)

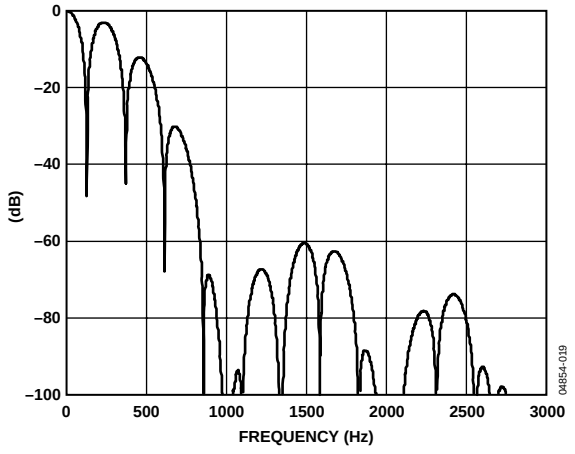

Figure 15. Filter Profile with Update Rate = 250 Hz (Chop Enabled)

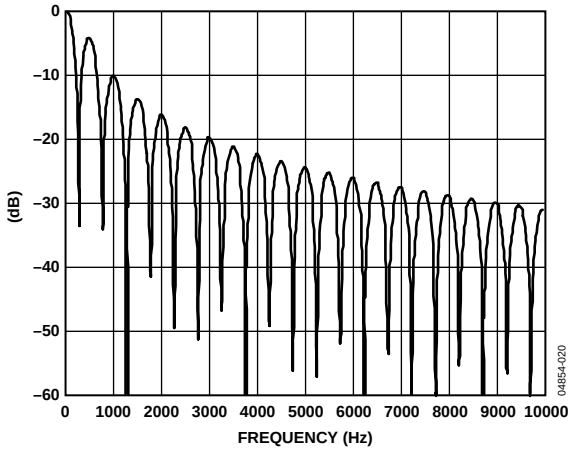

Figure 16. Filter Response at 500 Hz Update Rate (Chop Enabled)

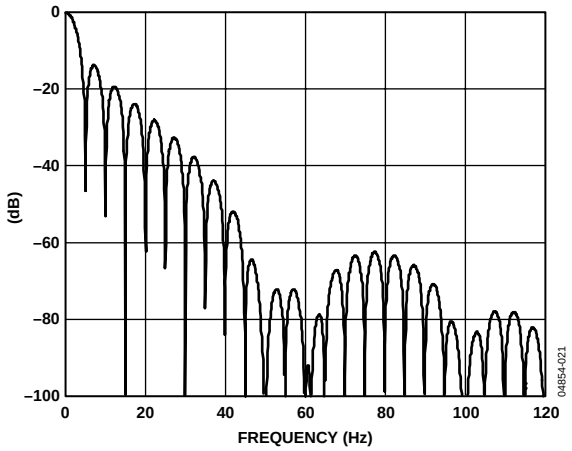

Figure 17. Filter Response at 4.17 Hz Update Rate (Chop Disabled)

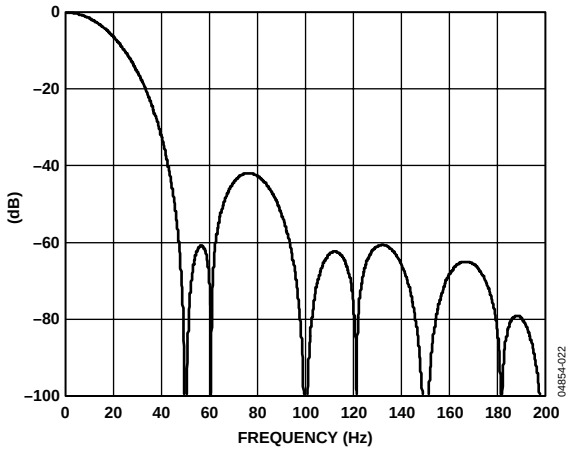

Figure 18. Filter Response at 16.7 Hz Update Rate (Chop Disabled)

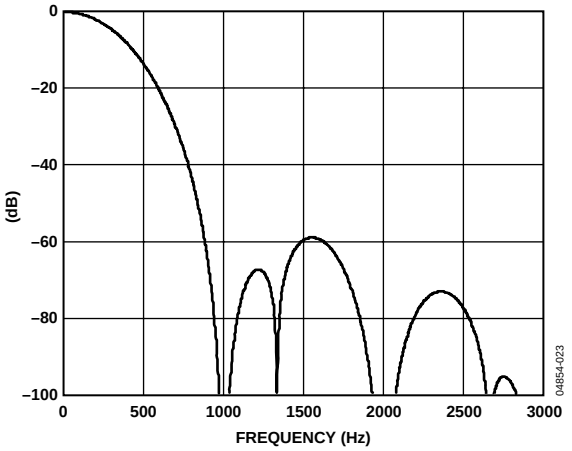

Figure 19. Filter Response at 250 Hz Update Rate (Chop Disabled)

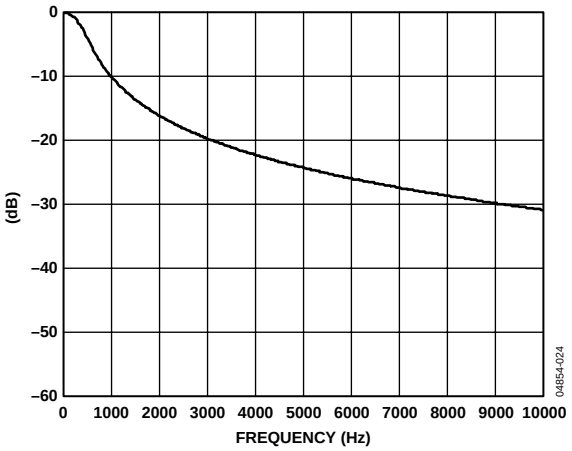

Figure 20. Filter Response at 500 Hz Update Rate (Chop Disabled)

DIGITAL INTERFACE

As previously outlined, the programmable functions of the AD7794 are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface, and read access to the on-chip registers is also provided by this interface. All communications with the part must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part begins with a write operation to the communications register, followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register, followed by a read operation from the selected register.

The serial interface of the AD7794 consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers, while DOUT/$\overline{RDY}$ is used for accessing from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT/$\overline{RDY}$) occur with respect to the SCLK signal. The DOUT/$\overline{RDY}$ pin operates as a data ready signal also, the line going low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the data register to indicate when not to read from the device, to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select a device. It can be used to decode the AD7794 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7794 with $\overline{CS}$ being used to decode the part. Figure 3 shows the timing for a read operation from the output shift register of the AD7794, while Figure 4 shows the timing for a write operation to the input shift register. It is possible to read the same word from the data register several times, even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations have been completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7794. The end of the conversion can be monitored using the $\overline{RDY}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idles high between data transfers.

The AD7794 can be operated with $\overline{CS}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$, because $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7794 line for at least 32 serial clock cycles, the serial interface is reset. This ensures that the interface can be reset to a known state if the interface gets lost due to a software error or some glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, the user should allow a period of 500 µs before addressing the serial interface.

The AD7794 can be configured to continuously convert or to perform a single conversion. See Figure 21 through Figure 23.

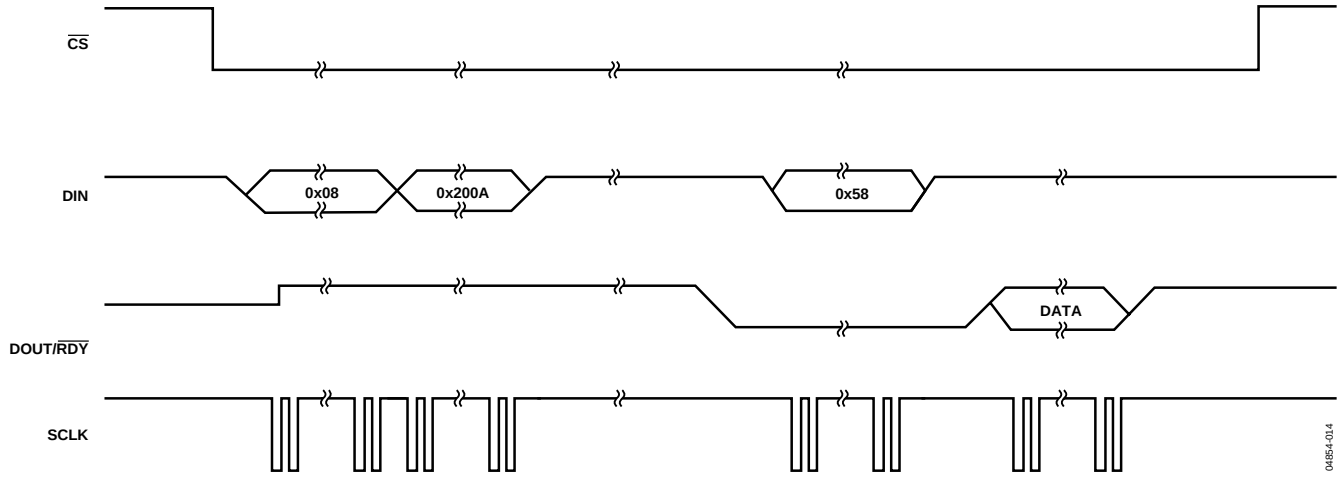

Figure 21. Single Conversion

Single Conversion Mode

In single conversion mode, the AD7794 is placed in shutdown mode between conversions. When a single conversion is initiated by setting MD2, MD1, MD0 to 0, 0, 1 in the mode register, the AD7794 powers up, performs a single conversion, and then returns to shutdown mode. The on-chip oscillator requires 1 ms to power up. A conversion will require a time period of 2 × t_{ADC}. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ will go high. If $\overline{CS}$ is low, DOUT/$\overline{RDY}$ will remain high until another conversion is initiated and completed. The data register can be read several times, if required, even when DOUT/ $\overline{RDY}$ has gone high.

Continuous Conversion Mode

This is the default power-up mode. The AD7794 continuously converts, the $\overline{RDY}$ pin in the status register going low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is completed. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. The digital conversion is placed on the DOUT/$\overline{RDY}$ pin as soon as SCLK pulses are applied to the ADC. DOUT/$\overline{RDY}$ returns high when the conversion is read. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion, or else the new conversion word is lost.

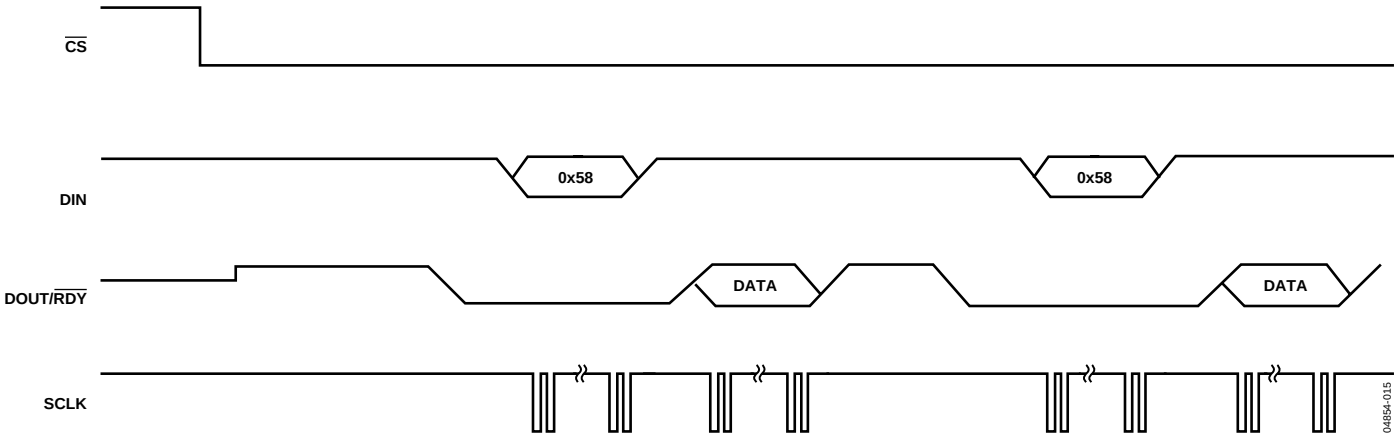

Figure 22. Continuous Conversion

Continuous Read

Rather than write to the communications register each time a conversion is complete to access the data, the AD7794 can be configured so that the conversions are placed on the DOUT/$\overline{\text{RDY}}$ line automatically. By writing 01011100 to the communications register, the user needs only to apply the appropriate number of SCLK cycles to the ADC, and the 24-bit word will be automatically placed on the DOUT/$\overline{\text{RDY}}$ line when a conversion is complete. The ADC should be configured for continuous conversion mode.

When DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC, and the data conversion will be placed on the DOUT/$\overline{\text{RDY}}$ line. When the conversion is read, DOUT/$\overline{\text{RDY}}$ returns high until the next conversion is available. In this mode, the data can be read only once. Also, the user must ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7794 to read the word, the serial output register is reset when the next conversion is complete and the new conversion is placed in the output serial register.

To exit the continuous read mode, the instruction 01011000 must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.

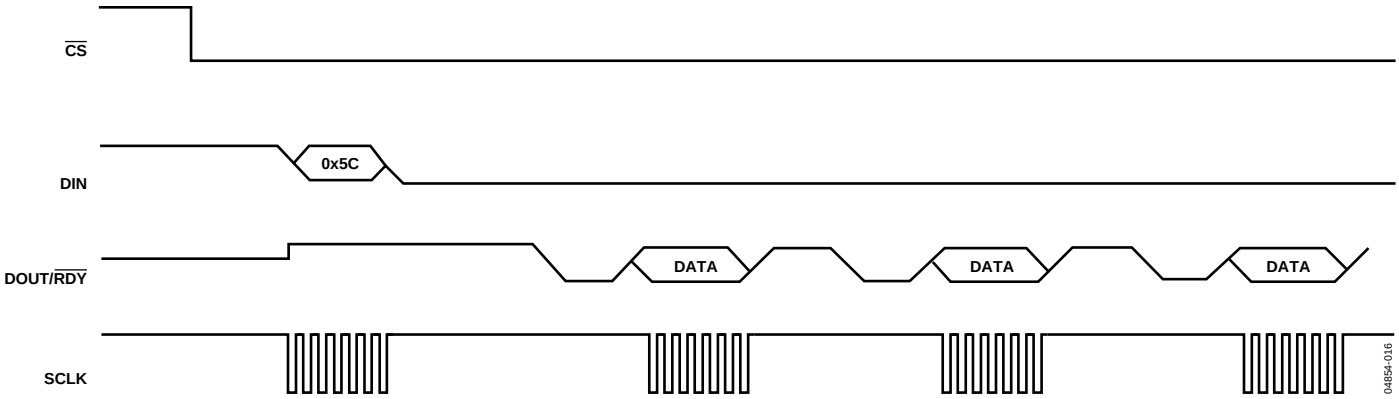

Figure 23. Continuous Read

CIRCUIT DESCRIPTION

ANALOG INPUT CHANNEL

The AD7794 has six differential analog input channels. These are connected to the on-chip buffer amplifier when the device is operated in buffered mode and directly to the modulator when the device is operated in unbuffered mode. In buffered mode (the BUF bit in the mode register is set to 1), the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors such as strain gauges or resistance temperature detectors (RTDs).

When BUF = 0, the part is operated in unbuffered mode. This results in a higher analog input current. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause gain errors, depending on the output impedance of the source that is driving the ADC input. Table 19 shows the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 20-bit level is introduced.

Table 19. External R-C Combination for No 20-Bit Gain Error

C (pF)	R (Ω)
50	9 k
100	6 k
500	1.5 k
1000	900
5000	200

The AD7794 can be operated in unbuffered mode only when the gain equals 1 or 2. At higher gains, the buffer is automatically enabled. The absolute input voltage range in buffered mode is restricted to a range between GND + 100 mV and AV_{DD} – 100 mV. When the gain is set to 4 or higher, the in-amp is enabled. The absolute input voltage range when the in-amp is active is restricted to a range between GND + 300 mV and AV_{DD} – 1.1 V. Care must be taken in setting up the common-mode voltage so that these limits are not exceeded. Otherwise, there will be degradation in linearity and noise performance.

The absolute input voltage in unbuffered mode includes the range between GND – 30 mV and AV_{DD} + 30 mV as a result of being unbuffered. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

INSTRUMENTATION AMPLIFIER

Amplifying the analog input signal by a gain of 1 or 2 is performed digitally within the AD7794. However, when the gain equals 4 or higher, the output from the buffer is applied to the input of the on-chip instrumentation amplifier. This low noise in-amp means that signals of small amplitude can be gained within the AD7794 while still maintaining excellent noise performance. For example, when the gain is set to 64, the rms noise is 40 nV typically, which is equivalent to 21 bits effective resolution or 18.5 bits peak-to-peak resolution.

The AD7794 can be programmed to have a gain of 1, 2, 4, 8, 16, 32, 64, and 128 using Bit G2 to Bit G0 in the configuration register. Therefore, with an external 2.5V reference, the unipolar ranges are from 0 mV to 20 mV to 0 V to 2.5 V while the bipolar ranges are from ±20 mV to ±2.5 V. When the in-amp is active (Gain ≥ 4), the common-mode voltage ((AIN(+) + AIN(−))/2) must be greater than or equal to 0.5 V when chopping is enabled. With chopping disabled, and with the AMP-CM bit set to 1 to prevent degradation in the common-mode rejection, the allowable common-mode voltage is limited to between

$$0.2 + (Gain/2 \times (AIN(+) - AIN(-)))$$

and

$$AV_{DD} - 0.2 - (Gain/2 \times (AIN(+) - AIN(-)))$$

If the AD7794 is operated with an external reference that has a value equal to AV_{DD}, for correct operation the analog input signal must be limited to 90% of V_{REF}/gain when the in-amp is active.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7794 can accept either unipolar or bipolar input voltage ranges. A bipolar input range does not imply that the part can tolerate negative voltages with respect to system GND. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the AIN(−) input. For example, if AIN(−) is 2.5 V and the ADC is configured for unipolar mode with a gain of 1, the input voltage range on the AIN(+) pin is 2.5 V to 5 V.

If the ADC is configured for bipolar mode, the analog input range on the AIN(+) input is 0 V to 5 V. The bipolar/unipolar option is chosen by programming the B/U bit in the configuration register.

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00...00, a midscale voltage resulting in a code of 100...000, and a full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = (2^N \times AIN \times GAIN)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN \times GAIN/V_{REF}) + 1]$$

where *AIN* is the analog input voltage, *GAIN* is the in-amp setting (1 to 128), and $N = 24$.

BURNOUT CURRENTS

The AD7794 contains two 100 nA constant current generators, one sourcing current from AV_{DD} to AIN(+), and one sinking current from AIN(−) to GND. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the burnout current enable (BO) bit in the configuration register. These currents can be used to verify that an external transducer is still operational before attempting to take measurements on that channel. Once the burnout currents are turned on, they will flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resultant voltage measured is full scale, the user needs to verify why this is the case. A full-scale reading could mean that the front end sensor is open circuit. It could also mean that the front end sensor is overloaded and is justified in outputting full scale, or the reference may be absent and the NOXREF bit is set, thus clamping the data to all 1s.

When reading all 1s from the output, the user needs to check these three cases before making a judgment. If the voltage measured is 0 V, it may indicate that the transducer has short circuited. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit in the configuration register. The current sources work over the normal absolute input voltage range specifications with buffers on.

EXCITATION CURRENTS

The AD7794 also contains two matched, software configurable constant current sources that can be programmed to equal 10 μA, 210 μA or 1 mA. Both source currents from AV_{DD} are directed to either IOUT1 or IOUT2 pins of the device. These current sources are controlled via bits in the IO register. The configuration bits enable the current sources and direct the current sources to IOUT1 or IOUT2, along with selecting the value of the current. These current sources can be used to excite external resistive bridge or RTD sensors.

BIAS VOLTAGE GENERATOR

A bias voltage generator is included on the AD7794. This will bias the negative terminal of the selected input channel to $AV_{DD}/2$. This function is available on inputs AIN1 to AIN3. It is useful in thermocouple applications, as the voltage generated by the thermocouple must be biased about some dc voltage if the gain is greater than 2. This is necessary because the instrumentation amplifier requires headroom, because signals close to GND or AV_{DD} will not be converted accurately.

The bias voltage generator is controlled using the VBIAS1 and VBIAS0 bits in conjunction with the boost bit in the configuration register. The power up time of the bias voltage generator is dependent on the load capacitance. To accommodate higher load capacitances, the AD7794 has a boost bit. When this bit is set to 1, the current consumed by the bias voltage generator is increased so that the power up time is considerably reduced. Figure 11 shows the power up times when boost equals 0 and 1 for different load capacitances. The current consumption of the AD7794 increases by 40 μA when the bias voltage generator is enabled, and boost equals 0. With the boost function enabled, the current consumption increases by 250 μA.

REFERENCE

The AD7794 has an embedded 1.17 V reference. This reference can be used to supply the ADC or an external reference can be applied. The embedded reference is a low noise, low drift reference, the drift being 4 ppm/°C typically. For external references, the ADC has a fully differential input capability for the channel. In addition, the user has the option of selecting one of two external reference options (REFIN1 or REFIN2). The reference source for the AD7794 is selected using the REFSEL1 and REFSEL0 bits in the configuration register. When the internal reference is selected, it is internally connected to the modulator (it is not available on the REFIN pins).

The common-mode range for these differential inputs is from GND to AV_{DD}. The reference input is unbuffered; therefore, excessive R-C source impedances will introduce gain errors. The reference voltage REFIN (REFIN(+) − REFIN(−)) is 2.5 V nominal, but the AD7794 is functional with reference voltages from 0.1 V to AV_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source will be removed, because the application is ratiometric. If the AD7794 is used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7794 include the ADR381 and ADR391, which are low noise, low power references. Also note that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source driving the reference inputs.

Reference voltage sources like those recommended above (for example, ADR391) will typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on

REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN pins is not recommended in this type of circuit configuration.

REFERENCE DETECT

The AD7794 includes on-chip circuitry to detect if the part has a valid reference for conversions or calibrations if the user selects an external reference as the reference source. This feature is enabled when the REF-DET bit in the configuration register is set to 1. If the voltage between the selected REFIN(+) and REFIN(–) pins goes below 0.3 V or either the REFIN(+) or REFIN(–) inputs are open circuit, the AD7794 detects that it no longer has a valid reference. In this case, the NOXREF bit of the status register is set to 1. If the AD7794 is performing normal conversions and the NOXREF bit becomes active, the conversion results revert to all 1s. Therefore it is not necessary to continuously monitor the status of the NOXREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC's data register is all 1s. If the AD7794 is performing either an offset or full-scale calibration and the NOXREF bit becomes active, the updating of the respective calibration registers is inhibited to avoid loading incorrect coefficients to these registers, and the ERR bit in the status register is set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR bit should be checked at the end of the calibration cycle.

RESET

The circuitry and serial interface of the AD7794 can be reset by writing 32 consecutive 1s to the device. This will reset the logic, the digital filter, and the analog modulator, while all on-chip registers are reset to their default values. A reset is automatically performed on power up. When a reset is initiated, the user must allow a period of 500 μs before accessing any of the on-chip registers. A reset is useful if the serial interface becomes asynchronous due to noise on the SCLK line.

AV_{DD} MONITOR

Along with converting external voltages, the ADC can be used to monitor the voltage on the AV_{DD} pin. When Bit CH2 to Bit CH0 equals 1, the voltage on the AV_{DD} pin is internally attenuated by 6, and the resultant voltage is applied to the Σ-Δ modulator using an internal 1.17 V reference for analog to digital conversion. This is useful because variations in the power supply voltage can be monitored.

CALIBRATION

The AD7794 provides four calibration modes that can be programmed via the mode bits in the mode register. These are internal zero-scale calibration, internal full-scale calibration, system zero-scale calibration and system full-scale calibration, which will effectively reduce the offset error and full-scale error to the order of the noise. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register. The offset calibration coefficient is subtracted from the result prior to multiplication by the full-scale coefficient.

To start a calibration, write the relevant value to the MD2 to MD0 bits in the mode register. After the calibration is completed, the contents of the corresponding calibration registers are updated, the $\overline{RDY}$ bit in the status register is set, the DOUT/ $\overline{RDY}$ pin goes low (if $\overline{CS}$ is low), and the AD7794 reverts to idle mode.

During an internal zero-scale or full-scale calibration, the respective zero input and full-scale input are automatically connected internally to the ADC input pins. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the ADC pins before initiating the calibration mode. In this way, external ADC errors are removed.

From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration, if required, should always be performed before a full scale calibration. System software should monitor the $\overline{RDY}$ bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of calibration via a polling sequence or an interrupt-driven routine.

With chopping enabled, both an internal offset calibration and a system offset calibration take two conversion cycles. With chopping enabled, an internal offset calibration is not needed, as the ADC itself removes the offset continuously. With chopping disabled, an internal offset calibration or system offset calibration takes one conversion cycle to complete. Internal offset calibrations are required with chopping disabled and should occur before the full-scale calibration.

To perform an internal full-scale calibration, a full-scale input voltage is automatically connected to the selected analog input for this calibration. When the gain equals 1, a calibration takes two conversion cycles to complete when chopping is enabled and one conversion cycle when chopping is disabled. For higher gains, four conversion cycles are required to perform the full-scale calibration when chopping is enabled and two conversion cycles when chopping is disabled. DOUT/$\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. Internal full-scale calibrations cannot be performed when the gain equals 128. With this gain setting, a system full-scale calibration can be performed. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.

An internal full-scale calibration can be performed at specified update rates only. For gains of 1, 2, and 4, an internal full-scale calibration can be performed at any update rate. However, for higher gains, internal full-scale calibrations can be performed only when the update rate is less than or equal to 16.7 Hz, 33.3Hz, and 50 Hz. However, the full-scale error does not vary with update rate, so a calibration at one update is valid for all update rates (assuming the gain or reference source is not changed).

A system full-scale calibration takes two conversion cycles to complete, irrespective of the gain setting when chopping is enabled and one conversion cycle when chopping is disabled. A system full-scale calibration can be performed at all gains and all update rates. With chopping disabled, the offset calibration (internal or system offset) should be performed before the system full-scale calibration is initiated.

GROUNDING AND LAYOUT

Because the analog inputs and reference inputs of the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The digital filter will provide rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7794 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7794 is so high, and the noise levels from the AD7794 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7794 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes, because it gives the best shielding.

It is recommended that the GND pin of the AD7794 be tied to the AGND plane of the system. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The ground plane of the AD7794 should be allowed to run under the AD7794 to prevent noise coupling. The power supply lines to the AD7794 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. AV_{DD} should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to GND. DV_{DD} should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to the system's DGND plane, with the system's AGND to DGND connection being close to the AD7794. To achieve the best from these decoupling components, they should be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

APPLICATIONS

The AD7794 provides a low-cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, it makes the part more immune to noisy environments, making it ideal for use in sensor measurement and industrial and process control applications.

FLOWMETER

Figure 24 shows the AD7794 being used in a flowmeter application that consists of two pressure transducers, the rate of flow being equal to the pressure difference. The pressure transducers shown are the BP01 from Sensym. The pressure transducers are arranged in a bridge network and give a differential output voltage between its OUT+ and OUT– terminals. With rated full-scale pressure (in this case 300 mmHg) on the transducer, the differential output voltage is 3 mV/V of the input voltage (that is, the voltage between the IN(+) and IN(–) terminals).

Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 15 mV. The excitation voltage for the bridge can be used to directly provide the reference for the ADC, as the reference input range includes the supply voltage.

A second advantage of using the AD7794 in transducer-based applications is that the low-side power switch can be fully utilized in low power applications. The low-side power switch is connected in series with the cold side of the bridges. In normal operation, the switch is closed, and measurements can be taken. In applications where power is of concern, the AD7794 can be placed in standby mode, thus significantly reducing the power consumed in the application. In addition, the low-side power switch can be opened while in standby mode, thus avoiding unnecessary power consumption by the front-end transducers. When the part is taken out of standby mode, and the low-side power switch is closed, the user should ensure that the front-end circuitry is fully settled before attempting a read from the AD7794.

In the diagram, temperature compensation is performed using a thermistor. The on-chip excitation current supplies the thermistor. In addition, the reference voltage for the temperature measurement is derived from a precision resistor in series with the thermistor. This allows a ratiometric measurement so that variation of the excitation current has no affect on the measurement (it is the ratio of the precision reference resistance to the thermistor resistance that is measured).

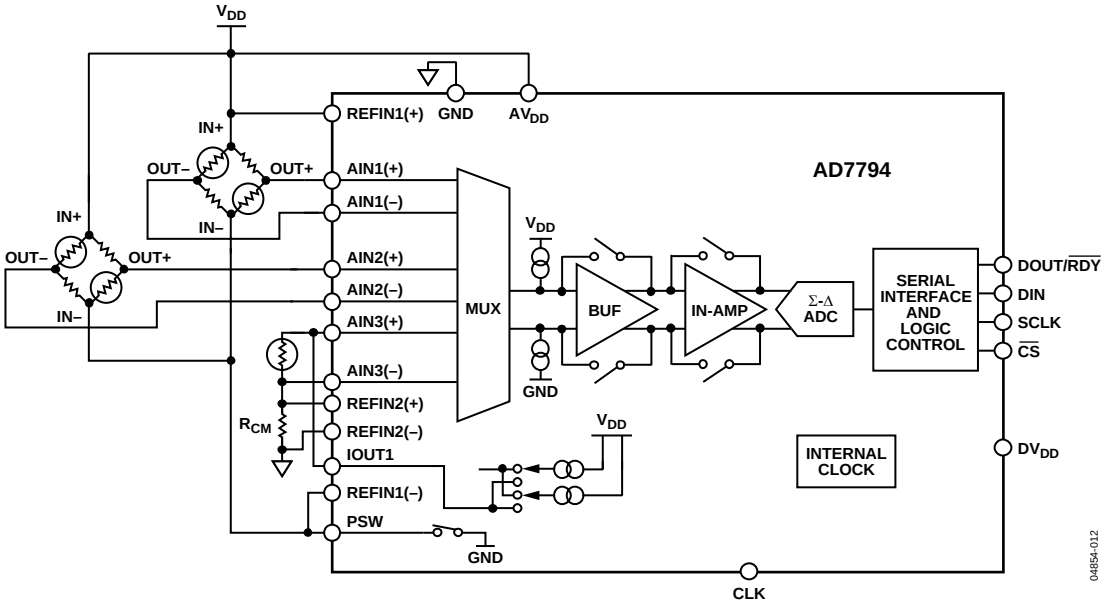

Figure 24. Typical Application (Flowmeter)

OUTLINE DIMENSIONS

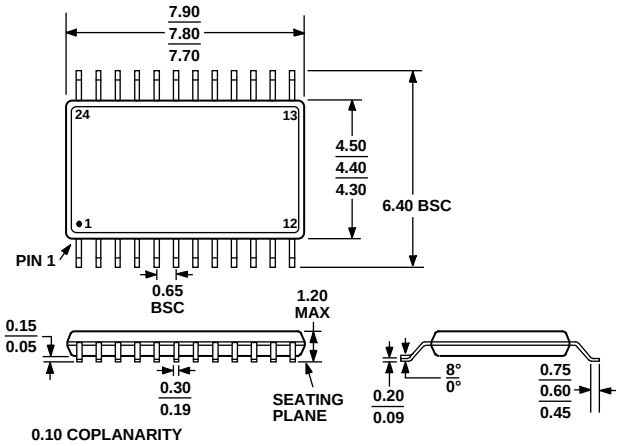

Figure 25. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option
AD7794BRU	–40°C to +105°C	24-Lead TSSOP	RU-24
AD7794BRU-REEL	–40°C to +105°C	24-Lead TSSOP	RU-24
AD7794BRUZ[1]	–40°C to +105°C	24-Lead TSSOP	RU-24
AD7794BRUZ-REEL[1]	–40°C to +105°C	24-Lead TSSOP	RU-24
EVAL-AD7794EB		Evaluation Board	

[1] Z = Pb-free part.

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